REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application and indicating that claims 2, 6, and 10 contain allowable subject matter. Further, Applicant thanks the Examiner for the courtesies extended in the telephonic Examiner Interview of November 16, 2004.

I. Disposition of Claims

Claims 1-10 and 13-15 are currently pending in the present application. By the way of this reply, claims 1, 5, 9, and 13 have been amended.

II. Claim Amendments

Claims 1, 5, 9, and 13 have been amended to clarify that a signal from an output of a clock driver residing outside a region of a clock grid is directly propagated past an exterior region of the clock grid to a connection point in a non-exterior region of the clock grid. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 4a, 4b, and 5 of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1, 3-5, 7-9, and 13-15 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0074642 in the name of Haritsa et al. (hereinafter "Haritsa"). For the reasons set

forth below, this rejection is respectfully traversed.

The present invention is generally directed to a integrated circuit design for reducing clock skew. A design in accordance with the present invention uses a clock driver disposed outside a region of a clock grid to drive a clock signal to clock grid connection points residing at non-exterior regions of the clock grid. While in prior art implementations as shown in Figures 3a – 3c of the present application, outputs of clock headers **40** are directly connected by interconnect **44** to exterior regions of a clock grid **42**, in exemplary embodiments of the present invention as shown in Figures 4a, 4b, and 5 of the present application, outputs of clock headers **40** are *directly connected* by interconnect **46** to non-exterior regions of a clock grid **42**. Accordingly, amended independent claims 1, 5, 9, and 13 of the present application require, in part, the direct propagation of a signal from an output of a clock driver (residing outside a clock grid) past an exterior region of the clock grid to a connection point in a non-exterior region of the clock grid.

Haritsa, on the other hand, fails at least to disclose those limitations of the claimed invention discussed above. Haritsa, which discloses a method for determining clock circuitry parameters in an integrated circuit design (*see* Haritsa, Abstract), fails to disclose the direct connection of an output of a clock driver outside a region of a clock grid to a non-exterior region of the clock grid. Figures 3 and 4 of Haritsa shows clock headers (e.g., **L2**) having outputs that are connected to exterior regions of a clock grid, similar to that shown in Figures 3a – 3c of the present application.

In view of the above, amended independent claims 1, 5, 9, and 13 of the present application are patentable over Haritsa. Dependent claims are allowable for at least the

same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.136001; P6821).

Respectfully submitted,

Date: 12/17/04

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